REMARKS

Claims 1 through 15 are currently pending in the application.

Claims 1, 4-9, and 11-15 stand rejected.

Claims 2, 3, and 10 are objected to.

Letter to the Chief Draftsman

Applicant submits herewith, under cover of a separate Letter to the Chief Draftsman, proposed corrections to FIG. 6 of the drawings. All proposed corrections have been marked in red. Applicant respectfully requests approval of the corrections to the drawings and will file corrected formal drawings upon receipt of such approval and a Notice of Allowance and Issue Fee Due in the application.

Information Disclosure Statement

Applicant notes the filing of an Information Disclosure Statement herein on June 19, 2002 and notes that a copy of the PTO-1449 was not returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

35 U.S.C. § 102 Anticipation Rejections

Claims 1, 4, 5, 7 and 9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yew et al. (U.S. Patent No. 6,049,129). Applicant respectfully traverses this rejection as hereinafter set forth.

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

By way of contrast with Yew et al. the embodiment of the presently claimed invention set forth in claim 1 recites elements of the invention calling for a semiconductor die comprising "a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface; at least on semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, having said at least one electrical connection area substantially aligned with said at least one semiconductor opening, said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device; at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening." Yew et al. does not disclose a direct electrical connection between the semiconductor die and the substrate. Yew discloses that electrical connections are

routed either through routing strips or through bus bars. Since Yew describes indirect connections through routing strips and bus bars Yew cannot describe "said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device".

As Yew et al. fails to expressly or inherently describe every element of claim 1, Applicant submits that claim 1 is not anticipated by Yew under 35 U.S.C. § 102.

Claims 4, 5, 7, and 9 are each allowable as depending either directly or indirectly from allowable claim 1.

35 U.S.C. § 103 Obviousness Rejections

Obviousness Rejection Based on U.S. Patent 6,049,129 to Yew et al.

Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. Applicant respectfully traverses this rejection as hereinafter set forth.

Applicants submit that M.P.E.P. § 706.2(j) sets forth the standard for a § 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic requirements must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The discussion of Yew above is incorporated herein by reference. Applicant respectfully submits that Yew fails to teach or suggest the elements of independent claim 15 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the elements of the claimed invention of a computer assembly comprising at least one semiconductor die assembly where the

semiconductor die assembly includes "said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device". Yew teaches that electrical connections are made through routing strips and bus bars as discussed above. Having failed to teach or suggest each and every limitation of presently amended independent claim 15, the cited prior art cannot and does not establish a *prima facie* case of obviousness regarding the claimed invention.

Applicant submits that the reference teaches away from the presently claimed invention and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention. Yew teaches that semiconductor device 50 is attached to printed circuit board 70. Printed circuit board 70 is substantially the same size as semiconductor device 50. (Col. 2, lines 21-22). This sub-assembly is in turn mounted on a higher level assembly. The printed circuit board 70 contains the routing strips 82 and bus bars 110 that are electrically connected to the semiconductor device. It would not be obvious to use a method that provides only indirect electrical connections when direct electrical connections are desired. The indirect attachment taught by Yew would not be compatible with the visual inspection method possible with Applicant's inspection since the printed circuit board would complicate visual inspection. Furthermore, Yew does not provide a means for protecting the surface of the semiconductor substrate from filler particles present in the encapsulant since the tape is installed between the device and the printed circuit board and does not prevent the encapsulant from contacting the surface of the substrate.

Accordingly, Yew cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Obviousness Rejection Based on U.S. Patent 6,049,129 to Yew et al. in view of Admitted Prior Art FIG. 15 and U.S. Patent 5,148,266 to Khandros et al.

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. in view of Admitted Prior Art (Fig. 15) and Khandros et al. (U.S. Patent No. 5,148,266).

The discussion of Yew et al. above, is incorporated herein by reference.

The Admitted Prior Art FIG. 15 illustrates chip-on-board (COB) bonding. Semiconductor die 202 is back-bonded with an adhesive layer 204 to a semiconductor substrate 206. The semiconductor die 202 is in electrical communication with the semiconductor substrate 206 through electrical elements extending between bond pads 208 on semiconductor die 202 and traces 212 on semiconductor substrate 206. The electrical connections are made using tape automated bonding (TAB) connectors 216. TAB connectors are generally metal leads carried on an insulating tape such as polyimide. The TAB connectors are attached to bond pads 208 on semiconductor die 202 and to a corresponding lead or trace 212 on semiconductor substrate 206. Encapsulant 218, typically a plastic resin, is used to cover the TAB connectors 218.

Khandros discloses a semiconductor chip assembly having an interposer and flexible leads (Title). The semiconductor chip is mounted to contact pads in a compact area array. An interposer is disposed between the chip and the substrate. The contacts on the chip are connected to terminals on the interposer by flexible leads that extend through openings in the interposer. (Abstract).

Applicant submits that the references themselves teach away from the proposed combination and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regrading the claimed invention. Yew teaches that the tape is used to adhere the semiconductor device to the printed circuit board. As discussed above, the tape does not protect the surface of the substrate from the filler particles present in the encapsulant. Additionally, Khandros teaches away from using TAB connections because the leads in TAB bonding extend beyond the chip in a radial pattern, resulting in a device much larger than the chip itself. Also, the leads are usually connected only to contacts at the periphery of the chip, thus rendering TAB connections

unsuitable for use where connections are to be made elsewhere on the chip.(Col. 3, lines 12-17). Therefore, it would not be obvious to combine a method for creating a substantially flat integrated circuit package having substantially the same outline as a chip with a connection method that results in a significantly larger package.

Accordingly, any combination of Yew, the Admitted Prior Art, and Khandros cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Obviousness Rejection Based on U.S. Patent 6,049,129 to Yew et al, in view of U.S. Patent 5,612,569 to Murakami et al.

Claim 8 rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. in view of Murakami et al. (U.S. Patent No. 5,612,569).

The discussion of Yew above, is incorporated herein by reference.

Murakami discloses a semiconductor device having bonding wires 5 covered with a flexible/fluid substance 20. Mold resin 2A covers flexible/fluid substance 20. The mold resin 2A is bored with a hole 22 at the side opposite to the principal surface of the semiconductor chip 1 to expose a portion of the semiconductor chip 1 to the outside. (FIG. 34, Col. 31, lines 13-17).

Applicant respectfully submits that Yew and Murakami fail to teach or suggest the elements of claim 8 to establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the elements of the claimed invention of the semiconductor die assembly of claim 7, further including "an encapsulant material encasing said at least one semiconductor die and said glob top material." Yew does not teach this limitation. Murakami teaches that the encapsulating material is bored with a hole to expose a portion of the semiconductor chip to the outside. To encase the semiconductor die the die must be completely covered, which is not possible if a hole is bored into the encapsulant.

Accordingly, any combination of Yew and Murakami cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

Obviousness Rejection Based on U.S. Patent 6,049,129 to Yew et al. view of U.S. Patent 4,784,782 to Boyko et al.

Claims 11 through 14 rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. in view of Boyko et al. (U.S. Patent No. 5,784,782).

The discussion of Yew et al. above is incorporated herein by reference.

Boyko discloses a method for fabricating printed circuit boards with cavities. The printed circuit board 10 has a dielectric layer 12 with metalizations 14 and 16 on both surfaces. (FIG. 1). The printed circuit board may have an additional dielectric layer 22, also with metalizations 24and 26 on both surfaces. (FIG. 1). A window 30 is cut in dielectric layer 22 to form a cavity 31. (FIG. 1). Sticker/adhesive sheet 40, which may be epoxy-glass or "pre-preg" is located between metallized dielectric sheets 12 and 22. (Col. 3, lines 35-38). Sticker/adhesive sheet 40 is designed for high flow when heat and pressure are applied. A window 44 is cut in sticker/adhesive sheet 40 and this window registers with window 30 in dielectric layer 22. (Col. 3, lines 38-44). A release layer 50 is placed on top of metallized dielectric layer 22. Layer 50 is highly stretchable and conformable. (Col. 3, lines 45-48). A sheet 60 of plug material 61 is laid on top of release layer 50. At room temperature, the plug material is pliable enough to tightly conform to cavity 31 and seal in sticker/adhesive sheet 40. (Col. 3, lines 60-62). Another non-melting release layer 70 is laid over sheet 60. Next, a breather layer 74 is laid over release layer 70. The resulting structure is sealed in a nylon bag, the bag is evacuated, and subjected to heat and pressure. (Col. 4, lines 21-29). When the release layer 70, sheet 74, are removed the resulting structure has the sticker/adhesive sheet bound ground plane 16 to metallized dielectric layer 22. The sticker/adhesive material has flowed within the cavity 31, creating a fillet 82 of the sticker/adhesive sheet material along the bottom perimeter of the cavity. (Col. 4, lines 32-39).

Applicant respectfully submits that Yew and Boyko fail to teach or suggest elements of claims 11 through 14 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the elements of the claimed invention of a semiconductor die assembly that includes

"at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor die" of claim11; "at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor substrate opening" of claim 12; "at least one fillet located proximate said at least one adhesive tape and said active surface of said at least one semiconductor die" of claim 13; and "at least one fillet located proximate said at least one adhesive tape and said semiconductor substrate first surface" of claim 14. Yew does not teach fillets. Boyko teaches fillets within a cavity formed in layers of a printed circuit board. The fillet material of Boyko is heated to liquify and settle at the bottom of the cavity to form fillets. Boyko does not teach or suggest that the fillet is proximate to adhesive tape, edge of semiconductor die, or substrate opening. Any semiconductor device mounted to the printed circuit board of Boyko would not be proximate to the fillets formed during the printed circuit board fabrication process since the fillets are formed at the bottom of the cavity, away from the mounting surface.

In addition, the references themselves teach away from the proposed combination and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention since Boyko is directed toward producing a printed circuit board with cavity. Yew teaches a chip size integrated package. It would not be obvious to combine a method for producing printed circuit board with cavities and a method for producing chip scale packages. Printed circuit board fabrication requires higher temperatures and pressures that would damage or destroy semiconductors.

Accordingly, any combination of Yew and Boyko cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Allowable Subject Matter

Claims 2, 3 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. Applicant has amended claims 2, 3, and 10 in independent form.

ENTRY OF AMENDMENT

Applicant requests entry of this amendment for the following reasons:

The amendment is timely filed.

The amendment reduces the number of issues for any subsequent appeal.

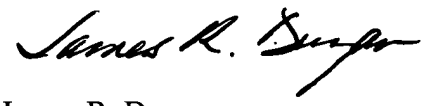
The amendment does not require any further search or consideration.

The amendment places the application in condition for allowance.

Applicant submits that claims 1 through 15 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 15 and the case passed for issue.

Respectfully submitted,



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Date: March 13, 2003

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Enclosure: Version with Markings to Show Changes Made

N:\2269\3818.1\Amendment 3.wpd

APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Five Times Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening.

2. (Twice Amended) [The semiconductor die assembly of claim 1,] A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening;

wherein said width of said at least one adhesive tape extends beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening.

3. (Twice Amended) [The semiconductor die assembly of claim 1,] A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical

connection area is directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening;

wherein said width of said at least one adhesive tape extends beyond said edge of said at least one semiconductor die a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface.

10. (Amended) [The semiconductor die assembly of claim 9,] A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening;

wherein said at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon; and

wherein a composition of said first adhesive differs from a composition of said second adhesive.

15. (Four Times Amended) A computer comprising:

at least one semiconductor die assembly, said semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; said electrical connection area disposed on said semiconductor die active surface wherein all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tongbi Jiang

Serial No.: 09/543,034

Filed: April 5, 2000

For: TAPE ATTACHMENT CHIP-ON-BOARD ASSEMBLIES

Examiner: D. Kang

Group Art Unit: 2811

Attorney Docket No.: 3818.1US (98-0887.1)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

March 13, 2003
Date of Deposit

Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Deidra Pfeil
Typed/printed name of person whose signature is contained above

LETTER TO THE CHIEF DRAFTSMAN

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant submits herewith revised FIG. 6 to correct errors in the drawing. Specifically, FIG. 6 has been revised to add encapsulant material 146 as claimed in claim 8.

No new matter has been added. Approval of the revised figures is respectfully requested.

Respectfully submitted,

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FIG. 6